

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 39

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HISANORI FUJISAWA

Appeal No. 2004-0636
Application No. 09/045,041

HEARD: November 18, 2004

Before FLEMING, GROSS, and MACDONALD, ***Administrative Patent Judges.***
GROSS, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 9 through 12, 14 through 24, 26 through 36, and 38 through 44, which are all of the claims pending in this application. On page 3 of the Answer, the examiner indicates that claims 19, 31, and 43 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Accordingly, only claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and 38 through 42, and 44 remain before us on appeal.

Appellant's invention relates to a method of carrying out simulation of a circuit. The method simplifies simulation by checking for partial circuits exhibiting equivalent operational characteristics and compressing such operationally equivalent partial circuits into one partial circuit. Claim 9 is illustrative of the claimed invention, and it reads as follows:

9. A method of carrying out simulation of a circuit, comprising:

inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

inspecting the plurality of partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, and judging equivalence when the configurations of said plurality of partial circuits are mutually consistent; and

compressing the circuit by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Chakrabarti et al., "An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-circuits," IEEE Proc Fourth Test Symp. 237-243 (1995)
(Chakrabarti)

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Claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and 38 through 42, and 44 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chakrabarti.¹

Reference is made to the Examiner's Answer (Paper No. 33, mailed August 12, 2003) for the examiner's complete reasoning in support of the rejections, and to appellant's Brief (Paper No. 31, filed May 22, 2003) and Reply Brief (Paper No. 34, filed October 14, 2003) for appellant's arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellant and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and 38 through 42, and 44. We also will enter a new ground of rejection under 35 U.S.C § 112, second paragraph, for claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32

¹ On pages 2-3 of the Answer, the examiner indicates that the rejections over Yokomizo, Filseth, Shinsha, Hachiya, Wang, and Kuehlmann have been withdrawn.

through 36, and 38 through 42, and 44 pursuant to 37 C.F.R.
§ 41.50(b).

Appellant (Brief, page 9) summarizes Chakrabarti as disclosing "**grouping together** identical gate-level **sub-circuits into high-level sub-circuits** based upon the characteristics of logical operations" (emphasis ours). Appellant asserts (Brief, page 10) that the present invention distinguishes over Chakrabarti in that "circuit simulation is performed by **integrating** a plurality of **partial circuits**, which are determined to exhibit equivalent operational characteristics, **into one partial circuit**" (emphasis ours).

First, we note that appellant's claims recite integrating into one circuit, but do not specify that the one circuit is one of the **partial** circuits. Thus, appellant's arguments are not commensurate in scope with the claims.

Second, appellant's argument focuses on the claim limitation of "integrating" plural partial circuits into one circuit. "To integrate" is defined as:²

1. To bring together or incorporate (parts) into a whole.

² Random House College Dictionary Revised Edition 692 (1982).

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2. To make up, combine, or complete to produce a whole or a larger unit, as parts do.

In other words, the ordinary meaning of integrating suggests making a bigger unit by bringing together multiple small units. There is a heavy presumption that words have the ordinary and customary meaning that would be attributed to those words by skilled artisans in the relevant art. **Texas Digital Systems Inc. v. Telegenix Inc.**, 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1817 (Fed. Cir. 2002), **quoting CCS Fitness, Inc. v. Brunswick Corp.**, 288 F.3d 1359, 1366, 62 USPQ2d 1658, 1662 (Fed. Cir. 2002).

"However, 'an inventor may choose to be his own lexicographer if he defines the specific terms used to describe the invention 'with reasonable clarity, deliberateness, and precision.'" *Teleflex*, 299 F.3d at 1325 (quoting *In re Paulsen*, 30 F.3d 1475, 1480 [31 USPQ2d 1671] (Fed. Cir. 1994)). 'Such a definition may appear in the written description or in the prosecution history.' *Teleflex*, 299 F.3d at 1325 (citations omitted)."

Golight Inc. v. Wal-Mart Stores Inc., 355 F.3d 1327, 1332, 69 USPQ2d 1481, 1485 (Fed. Cir. 2004). We find no such specific definition of "integrating." Thus, the portion of the claims relied upon in appellant's argument would appear to be met by appellant's summary of Chakrabarti, as Chakrabarti groups, or integrates, identical sub-circuits into a larger high-level sub-circuit.

However, appellant's claims actually recite compressing by integrating. We find the use of the word "integrating" to be inconsistent with the idea of compression. Appellant (Specification, page 4) defines "circuit compression" as "[c]onverting a circuit composed of a plurality of circuit elements and a plurality of terminals into a circuit having one simple circuit element and terminals." Appellant (Specification, page 4) explains that Figure 2(B) shows the compressed version of Figure 2(A), as the two identical partial circuits Q1 and Q2 of Figure 2(A) have been reduced to a single partial circuit in Figure 2(B). Similarly, appellant (Specification, page 26) explains that Figure 13 is a compressed form of Figure 11 in that "the numbers of circuit elements of the first partial circuit 31 and first partial circuit 32 shown in Figure 11 are compressed to half." Thus, "compressing the circuit," as recited in claim 9, for example, refers to reducing the number of partial circuits.

However, appellant recites in claim 9, for example, that the circuit is compressed by "integrating the partial circuits." As explained *supra*, integrating suggests making a bigger unit by bringing together multiple small units. Since compressing, as defined by appellant, means reducing the number of small units by eliminating the redundancies, thereby making a smaller unit, it

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is unclear how the circuit can be compressed by integrating the partial circuits. As we are unable to determine the metes and bounds of the claims, we would have to resort to speculation and assumptions to apply prior art to the above-noted limitations of the claims. **See In re Steele**, 305 F.2d 859, 862-63, 134 USPQ 292, 295 (CCPA 1962). Therefore, we cannot sustain the anticipation rejection of claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and 38 through 42, and 44 over Chakrabarti.

Under the provisions of 37 C.F.R. § 41.50(b), we enter the following new ground of rejection against appellant's claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and 38 through 42, and 44. Claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and 38 through 42, and 44 are rejected under 35 U.S.C. § 112, second paragraph, as being vague and indefinite substantially for the reasons explained **supra**.

CONCLUSION

The decision of the examiner rejecting claims 9 through 12, 14 through 18, 20 through 24, 26 through 30, 32 through 36, and

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38 through 42, and 44 under 35 U.S.C. § 102 is reversed and a new ground of rejection under 35 U.S.C. § 112, second paragraph, has been entered.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) (effective September 13, 2004, 69 Fed. Reg. 49960 (August 12, 2004), 1286 Off. Gaz. Pat. Office 21 (September 7, 2004)). 37 C.F.R. § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

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No time period for taking any subsequent action in
connection with this appeal may be extended under 37 C.F.R.
§ 1.136(a)(1)(iv).

REVERSED
37 C.F.R. § 41.50(b)



MICHAEL R. FLEMING
Administrative Patent Judge



ANITA PELLMAN GROSS
Administrative Patent Judge



ALLEN R. MACDONALD
Administrative Patent Judge

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